



Analyzing and Eliminating Die Passivation Crack in a Power Leadframe Package using Submodeling Approach

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Author's contribution

The author performed the thermomechanical simulation in this study and also read and reviewed the final manuscript.

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ABSTRACT

This paper presents the submodeling approach in thermo-mechanical simulation of the die passivation crack encountered in a power leadframe package subjected to temperature cycling condition. Without using modeling and simulation in resolving semiconductor package development issues, the process would be very costly and time-consuming. For die passivation crack, the details of the different layers of the die passivation need to be modeled and this would result in a large simulation model with considerable solution time. However, a technique known as submodeling can be used to reduce solution time without sacrificing accuracy of results. In this study, submodeling was successfully used to analyze the stresses in the critical passivation layer that resulted in the best design that eliminated the passivation crack. The modeling result showed that the crack could be eliminated by using the right passivation material layer combination and thickness. An increase in the thickness of the material layers and the additional of sublayers have provided significant stress reduction in the topmost critical passivation layer resulting in crack elimination.

Keywords: *Passivation crack; submodeling; thermal cycling; finite element analysis; power package.*

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1. INTRODUCTION

Leadframe-based packages for power device applications require higher thermal performance to dissipate heat generated in the silicon die. Leadframe die pad, the leadframe region under the die, has been used as a heat sink for removal of heat. However, as device power increases, the thermal requirement also increases. Recent direction is to use dual side cooling design in which the top side of the die also has heat sink in the form of an exposed copper clip as shown in Fig. 1. In this kind of power package, temperature cycling is a common reliability testing requirement. One of the reliability problems during temperature cycling of this package is the die passivation crack. The package materials used in this semiconductor package have different coefficient of thermal expansion (CTE). The crack is usually the result of excessive thermomechanical stress induced due to CTE mismatch.

The die passivation provides protection to the active circuit of the die or the metallization but passivation crack is still a common problem. In a study by Barti and Stecher [1], submodeling was also used to understand passivation cracks and the focus was on one semiconductor package with specific passivation design that had the passivation crack problem. Another investigation [2] tried to explain the mechanism of thin film cracking caused by temperature cycling and

focused mainly on silicon nitride (SiN) film. SiN is a very common passivation material used for microchips or integrated circuit (IC) die structures. There are other studies [1-2,4-8,10-11] related to passivation crack but they are mostly considering analysis on a single set of material and layer combination.

This study focuses on analyzing the stress levels in the critical die passivation layer of a power package in which crack was encountered and finding the best passivation design that provides lower stress to eliminate the crack problem. The different designs consist of different material combinations of the die passivation layers as well as different thickness values.

2. METHODOLOGY

2.1 Thermomechanical Simulation

In developing a semiconductor package, cost and lead time are some of the key factors that need to be considered. Thermomechanical simulation to analyze failures and explore design improvements is now commonly used because doing several evaluation trials with different package design and material combinations would take time and is very costly. Simulation is usually done using finite element analysis (FEA) technique where different “what if” scenarios or design options could be easily analyzed.

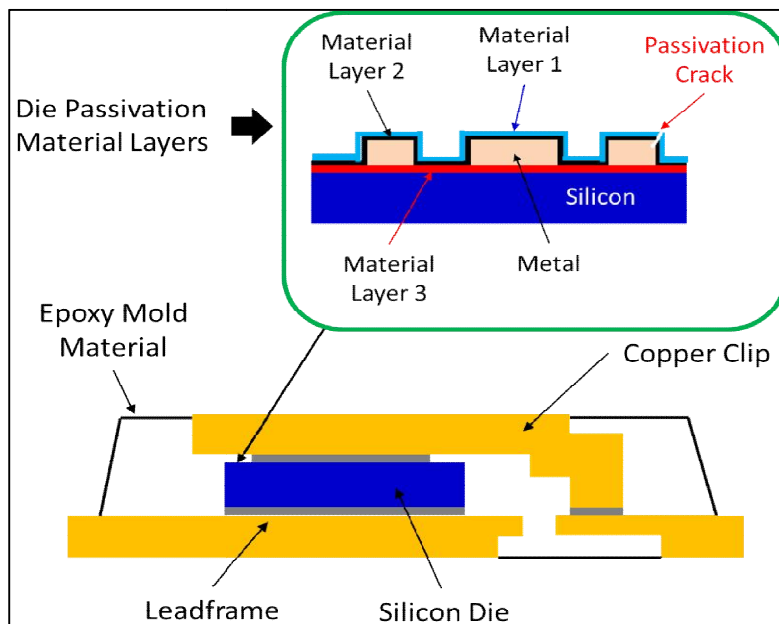


Fig. 1. Power package with copper clip showing detailed die passivation layers

2.1.1 Global modeling

In the global modeling, the whole package is considered. The mesh is coarse in the global model and package loadings are applied such as temperature in the thermal cycling conditions the package is subjected to. The model is then solved and a cut boundary is created from which displacement boundary conditions for the submodel would be extracted.

2.1.2 Submodeling

Submodeling, as discussed in [3,9], is a technique used in finite element analysis (FEA) that can be used to obtain more accurate results in a particular region of a model. A finite element mesh may be too coarse to produce satisfactory results in a given region of interest. Re-analyzing the entire model using finer mesh to obtain more accurate results is time-consuming and costly. Instead, submodeling can be used to generate an independent, more finely meshed model of only the region (submodel) of interest and analyze it. Submodeling is also known as the cut-boundary displacement method since the displacements on the coarse model's cut boundary are specified as boundary conditions for the submodel. This technique is based on St. Venant's principle, which states that if an actual distribution of forces is replaced by a statically equivalent system, the stress and strain distributions are altered only near the regions of load application. This means that a reasonably accurate results can be calculated in the submodel if its boundaries are far enough from the region where stress would be analyzed.

2.2 Power Package Die Passivation Modeling

In this study, the thermal cycling condition applied was $-55^{\circ}\text{C}/150^{\circ}\text{C}$. For the molded package, reference temperature or stress-free temperature was assumed to be 175°C , the same as the post mold cure (PMC) temperature. Stress level at -55°C (highest stress) was then simulated.

Linear elastic materials properties were used for all materials.

The finite element models in Fig. 2 are showing both the global model and the submodel. The submodel shown is like a refined zoom model, which includes the different layers of the die passivation. The submodel location identified is the active surface of the die near the die edge as this is the region where the passivation failure was encountered. The global model was solved first before proceeding with the submodel analysis. Nodal displacements from the initial/global model results were mapped to the cut boundaries of the submodel for subsequent multi-layer passivation stress analysis.

Table 1 shows the different passivation design options that were analyzed. Material layer thickness values are also listed in the table. Material 1 is the topmost passivation layer and this is the critical layer in this study. Some design options (New Designs 1,3,6) have another material sublayer below the topmost layer but still listed under Material 1. Material 2 is the layer below Material 1 and the thickness values are varied. The thickness of Material 3 is the same for all the designs.

3. RESULTS AND DISCUSSION

FEA result is shown in Fig. 3 for the topmost material layer (Material Layer 1) of the die passivation. A good agreement between the modeling result in terms of stress and actual failure location could be observed.

The normalized stress comparison for the different design options is shown in Fig. 4. The stress is normalized against the existing passivation design where the passivation crack problem was observed. It can be seen from the comparison that the increase in the thickness of the material layers helps reduce the stress in the topmost critical passivation layer. The layer thickness of Material 2 (from 0.3 to $1\ \mu\text{m}$ or higher) appears to be a significant contributor in reducing the stress of Material 1 layer. Actual evaluation of the best passivation design identified showed no passivation crack. This correlation between modeling result and actual result implies that the submodeling technique is a reliable method in analyzing and eliminating passivation crack by exploring some best design alternatives.

Table 1. Die passivation design options

Passivation design	Material 1 thickness	Material 2 thickness	Material 3 thickness
Existing design	0.7 μm	0.3 μm	0.9 μm
New design 1	0.3 μm / 0.15 μm	1.2 μm	0.9 μm
New design 2	0.9 μm	1.1 μm	0.9 μm
New design 3	0.3 μm / 0.15 μm	0.9 μm	0.9 μm
New design 4	0.6 μm	0.6 μm	0.9 μm
New design 5	1.0 μm	1.05 μm	0.9 μm
New design 6	0.6 μm / 0.5 μm	1.0 μm	0.9 μm
New design 7	0.55 μm	0.5 μm	0.9 μm

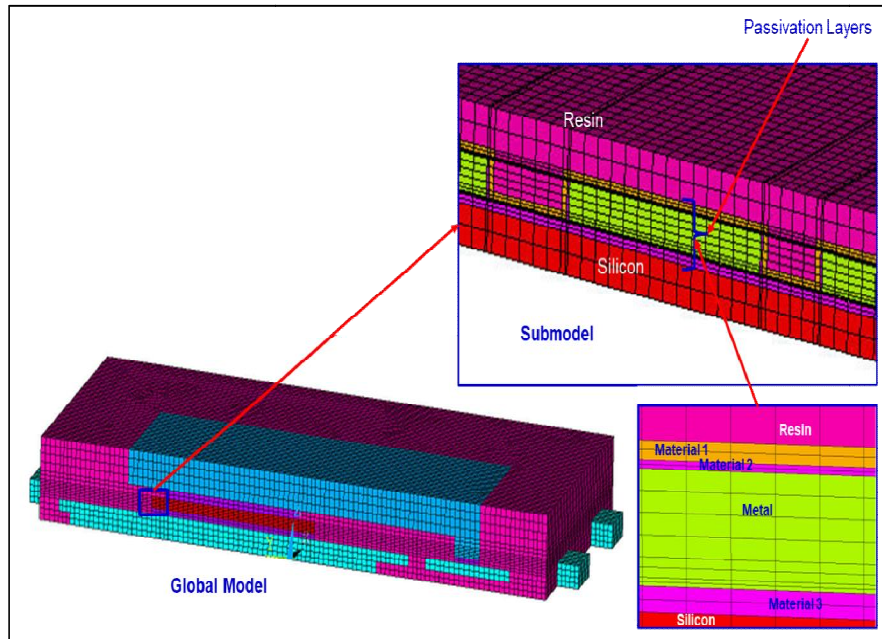


Fig. 2. Finite element model (global model and submodel)

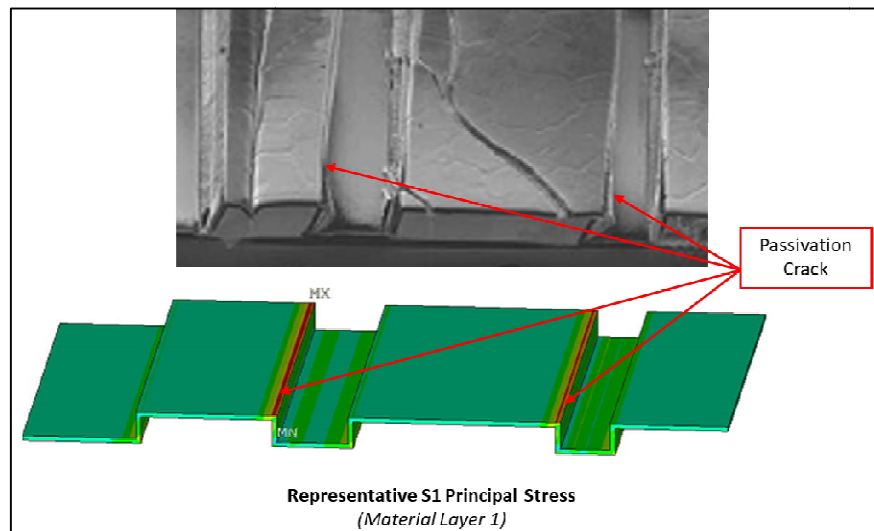


Fig. 3. Stress contour plot (passivation – material layer 1) vs actual crack

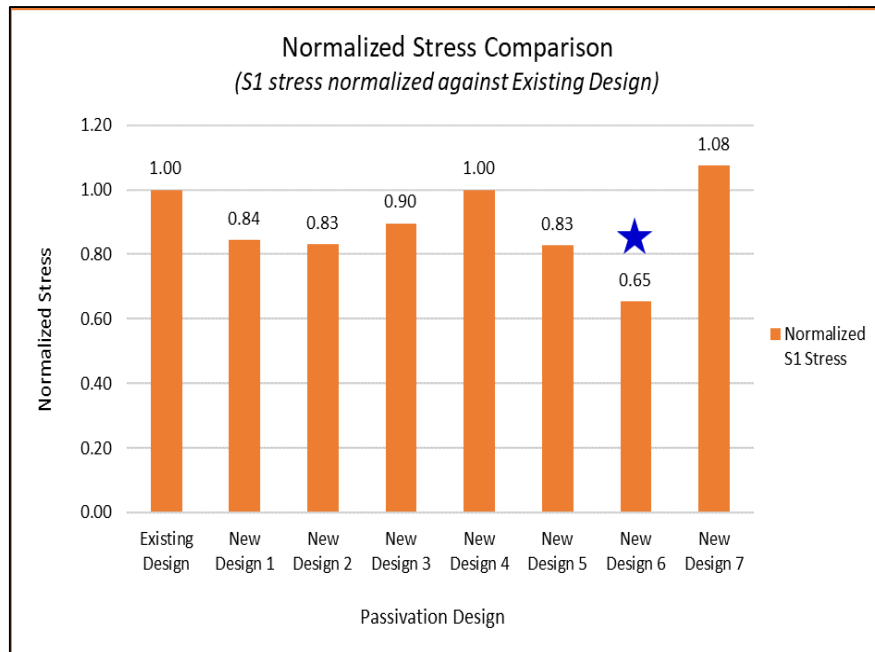


Fig. 4. Normalized stress comparison (die passivation layer)

4. CONCLUSION

Thermomechanical simulation was done on a power package with submodeling technique utilized to capture very small structural details of the different passivation layers and still consider the whole package response. Results showed that submodeling could be successfully used to analyze the stresses in the critical die passivation layer. From the results, the best design that eliminated the passivation crack was identified. It was also shown that the passivation crack could be eliminated by reducing the stress using the right passivation material layer combination and thickness. It was found out that an increase in the thickness of the material layers helps reduce the stress in the topmost critical passivation layer especially the material under the top critical layer appears to provide significant contribution. The addition of sublayers also shows some stress reduction.

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COMPETING INTERESTS

Author has declared that no competing interests exist. The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the author and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the author.

REFERENCES

1. Barti E, Stecher M. Using submodeling technique to understand passivation cracks in microelectronic devices. Proc. 2nd ANSA, ETA Int. Congr. 2007;241-256.
2. Huang M, Suo Z, Ma Q, Fujimoto H. Thin film cracking and ratcheting caused by temperature cycling. Journal of Materials Research. 2000;15(6):1239-1242.
3. ANSYS Manual, ANSYS Release 10.0; 2005.
4. Huang X, Zhu L, Nguyen B, Tran V, Isom H. Passivation stress versus top metal profiles by 3D finite element modeling. Proc CS MANTECH Conference; 2013.

5. He YT, Li HP, Shi R, Li F, Zhang GQ, Ernst LJ. Passivation cracking analyses of Micro-structures of IC packages. In Key Engineering Materials. 2006;324:515-518. Trans Tech Publications.
6. He YT, Van Gils MAJ, Van Driel WD, Zhang GQ, Van Silfhout RB, Ernst LJ. Prediction of crack growth in IC passivation layers. Microelectronics Reliability. 2004;44(12):2003-2009.
7. Van Silfhout RBR, van Driel WD, Li Y, van Gils MAJ, Janssen JHJ, Zhang GQ, Ernst LJ. Effect of metal layout design on passivation crack occurrence using both experimental and simulation techniques. In 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, 2004. EuroSimE 2004. Proceedings of the (2004, May). IEEE. 2004;69-74.
8. Prorok BC, Espinosa HD. Effects of nanometer-thick passivation layers on the mechanical response of thin gold films. Journal of Nanoscience and Nanotechnology. 2002;2(3-4);427-433.
9. Nayak R. Submodeling Technique in Stress Analysis. HCL Technologies; 2011.
10. Zhang XR, Zhu WH, Liew BP, Gaurav M, Yeo A, Chan KC. Copper pillar bump structure optimization for flip chip packaging with Cu/Low-K stack. In 2010 11th International Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE). IEEE. 2010;1-7.
11. Van Driel WD, Wisse G, Chang AY, Janssen JH, Fan X, Zhang KG, Ernst LJ. Influence of material combinations on delamination failures in a cavity-down TBGA package. IEEE Transactions on Components and Packaging Technologies. 2004;27(4):651-658.

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